

A Comparison of High-Level Full-System Power Models

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Talk Overview

- Power modeling goals and approaches
 - Models compared
 - Model generation and evaluation methodology
 - Evaluation results
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Who needs power models?

- Component and system designers
 - How do design decisions affect power?
 - Users
 - How do my usage patterns affect power?
 - Data center schedulers
 - How will workload distribution decisions affect power?
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Power modeling goals

- Goal: Online, full-system power models
 - Model requirements
 - Non-intrusive and low-overhead
 - Easy to develop and use
 - Fast enough for online use
 - Reasonably accurate (within 10%)
 - Inexpensive
 - Generic and portable
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Power modeling approaches

- Detailed component models
 - Simulation-based
 - Hardware metric-based

- **High-level full-system models**

High-level models (Mantis)

Input:
Common util. metrics

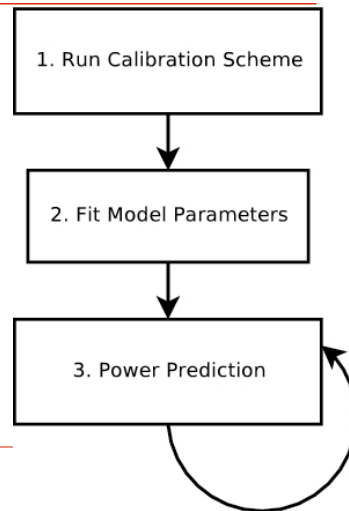
Equation →

Output:
Predicted power (system)

- How accurate?
 - How portable?
 - Tradeoff between model parameters/complexity and accuracy?
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Power Modeling

- Run **one-time** calibration scheme (possibly at vendor)
 - Stress individual components: CPU, memory, disk
 - *Outputs*: time-stamped performance metrics & AC power measurements
- Fit model parameters to calibration data
- Use model to predict power
 - Inputs: performance metrics at each time t
 - Output: estimation of AC power at each time t



Models studied

- Constant power (the null model): $P = C_0$

- CPU utilization-based models

Input:
CPU util. %

Equation →

Output:
Predicted power (system)

CPU utilization-based models

- Linear in CPU utilization

$$P = C_0 + C_1u$$

- Empirical power model

$$P = C_0 + C_1u + C_2u'$$

[Fan et al, ISCA 2007]

CPU + disk utilization

Input:

- CPU util. %
- Disk util. %

Equation



Output:

Predicted power (system)

$$P = C_0 + C_1u_{CPU} + C_2u_{disk}$$

[Heath et al, PPOPP 2005]

CPU + disk util. + performance ctrs

Input:

- CPU util. %
- Disk util. %
- CPU perfctrs

Equation



Output:

Predicted power (system)

$$P = C_0 + C_1u_{CPU} + C_2u_{disk} + \sum C_i P_i$$

[D. Economou, S. Rivoire, C. Kozyrakis, P. Ranganathan, MoBS 2006]

CPU performance counters

- Configurable processor registers to count microarchitectural events
 - In this study:
 - Memory bus transactions
 - Unhalted CPU clock cycles
 - Instructions retired/ILP
 - Last-level cache references
 - Floating-point instructions
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Evaluation methodology

- Run calibration suite and develop models on a variety of machines
 - Run benchmarks, collecting metrics and AC power
 - Compare predicted power from metrics with measured AC power
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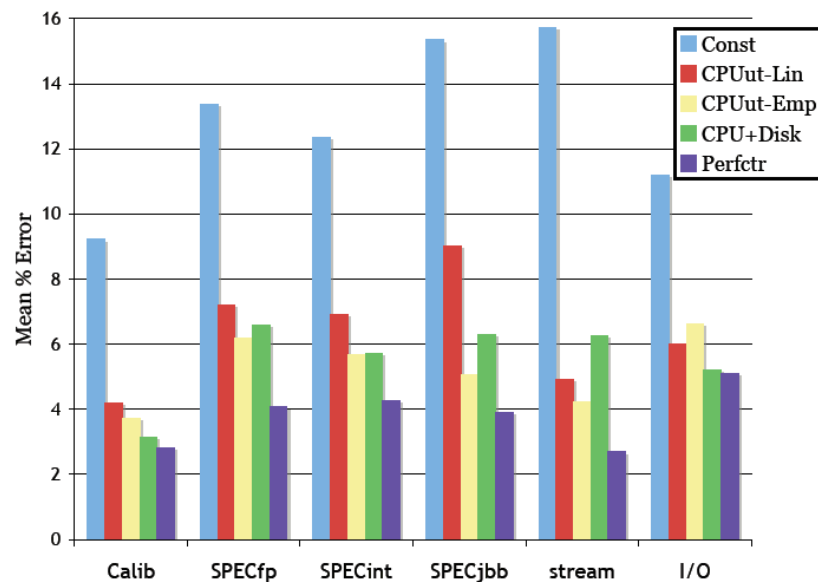
Evaluation benchmarks

- SPECcpu int and fp
 - Laptop: gcc and gromacs only
 - SPECjbb
 - Stream
 - I/O-intensive programs
 - ClamAV
 - Nsort (mobile fileserver only)
 - SPECweb (Itanium only)
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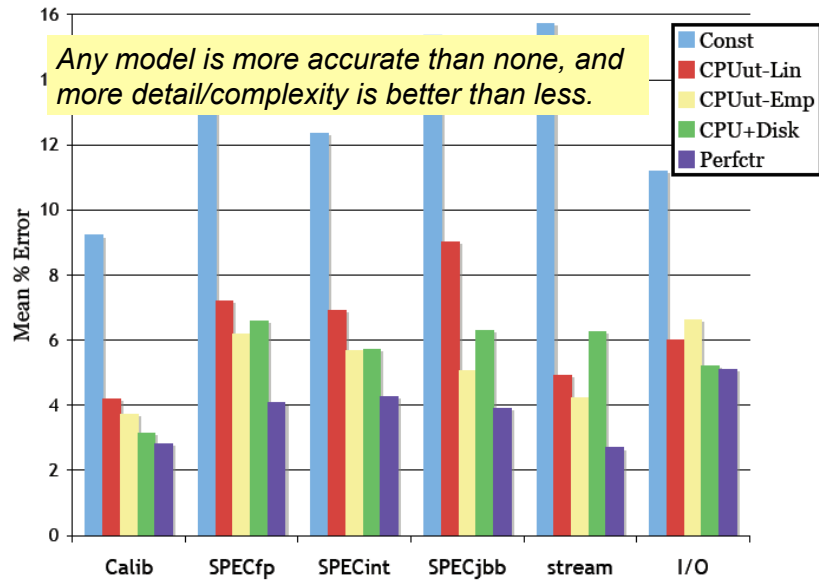
Evaluation machines

- Mobile fileserver with 1 and 13 disks
 - Highest and lowest frequencies
 - 2005-era AMD laptop
 - Highest and lowest frequencies
 - 2005-era Itanium server
 - 2008-era Xeon server with 32 GB FBDIMM
 - *Variety in component balance, processor, domain, dynamic range*
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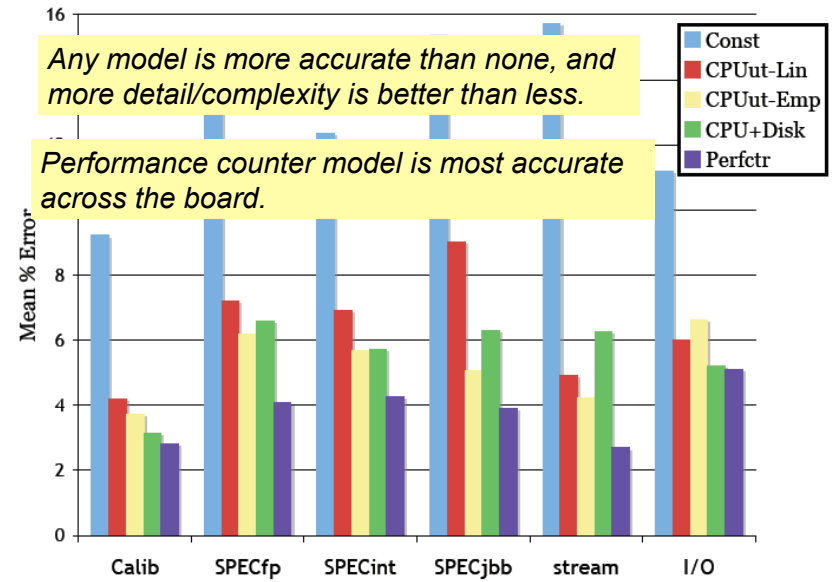
Overall mean % error



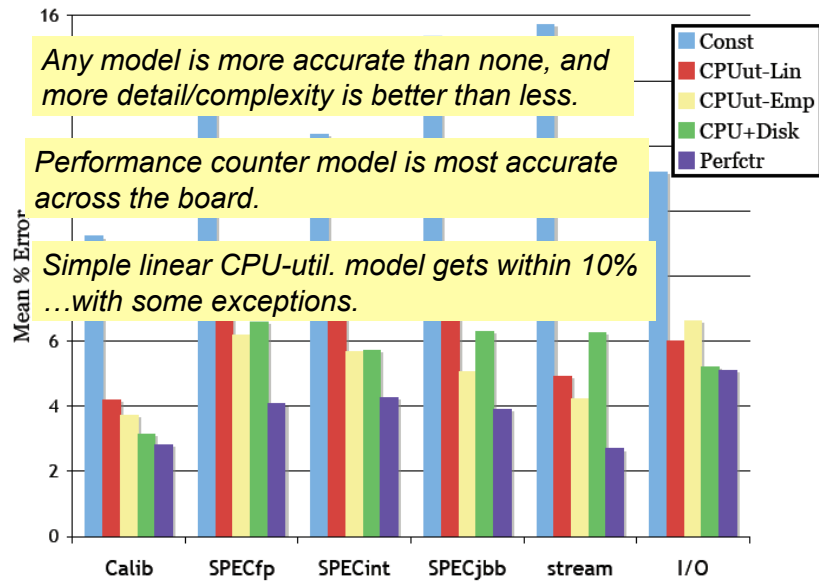
Overall mean % error



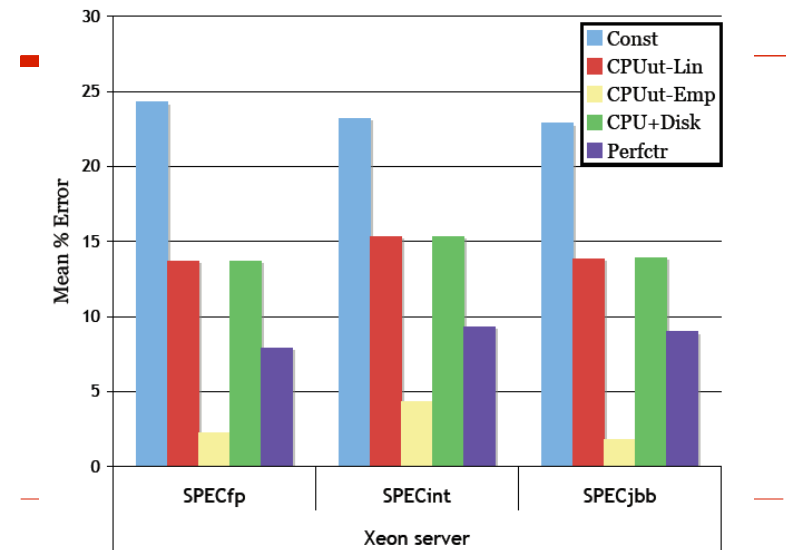
Overall mean % error



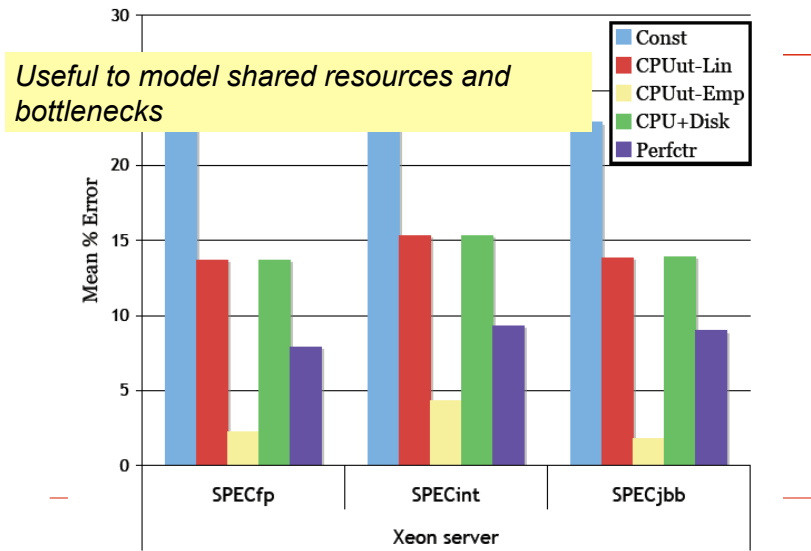
Overall mean % error



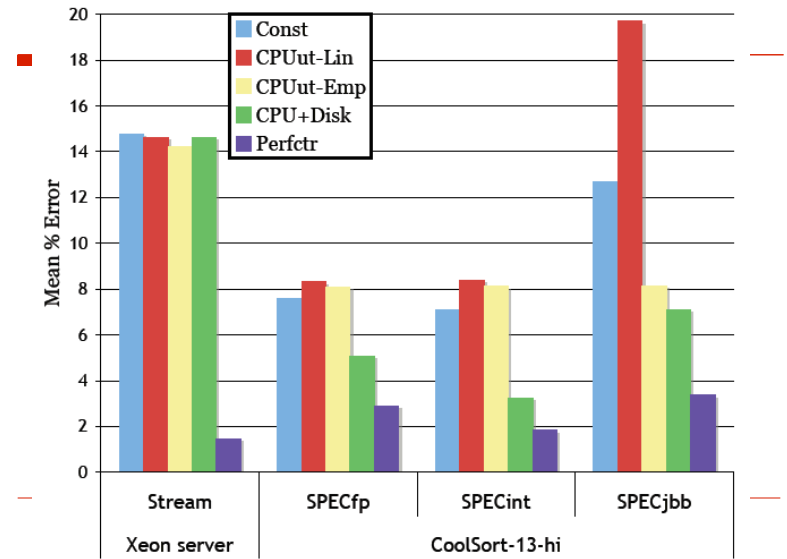
Best case for empirical CPU model (Xeon server)



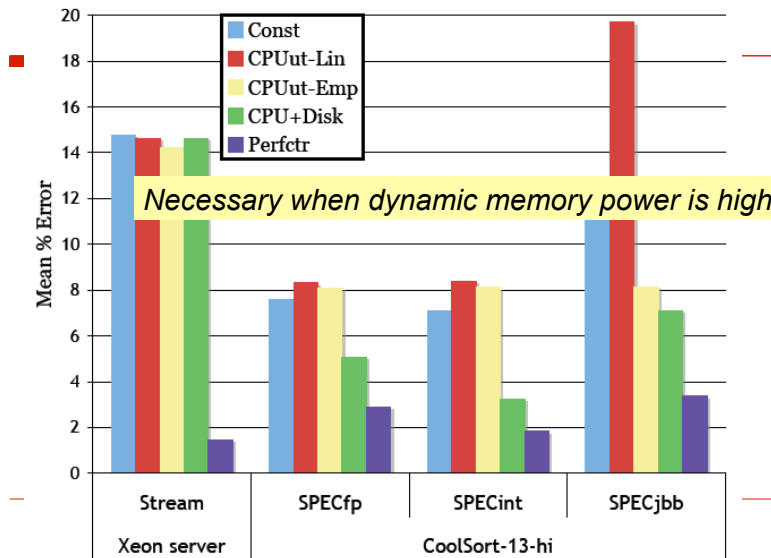
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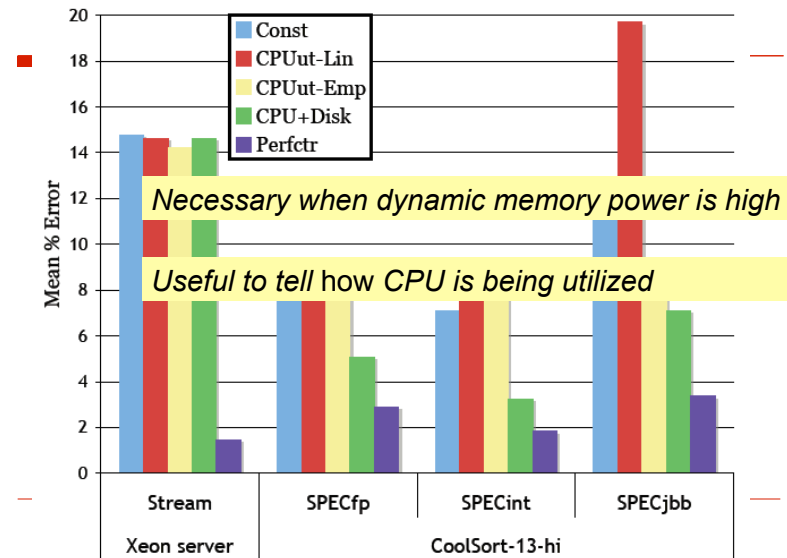
Best case for performance counters (Xeon server and mobile filesaver-13)



Best case for performance counters (Xeon server and mobile filesaver-13)



Best case for performance counters (Xeon server and mobile filesaver-13)



Future work

- Beyond CPU, memory, and disk
 - GPUs
 - Network (not a factor today)
 - Model complexity
 - Combine exponential CPU model w/ perfctrs?
 - Cooling – fan power is cubic function of speed
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Conclusions

- Generic approach to power modeling yields accurate results
 - Simple models overall have < 10% error
 - Same parameters across very different machines
 - More information → better models
 - Linear CPU util. model not enough for...
 - Machines and workloads that are not CPU-dominated
 - CPUs with shared resource bottlenecks
 - Aggressively power-optimized CPUs
 - ...*all of which reflect hardware trends.*
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